UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,781	07/25/2001	Jean Louis Calvignac	RAL920010025US1	5146

26675 7590 06/05/2007

DRIGGS, HOGG & FRY CO. L.P.A.
38500 CHARDON ROAD
DEPT. IRA
WILLOUGBY HILLS, OH 44094

EXAMINER	
MAIS, MARK A	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
06/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/912,781	CALVIGNAC ET AL.	
	Examiner	Art Unit	
	Mark A. Mais	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102/103

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Key et al. (USP 6,173,386) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Key et al. in view of Dockser et al (USP 5,860,119)

4. With regard to claim 21, Key et al. discloses a system for transmitting multiple frames **[Fig. 2, level 2/3 Router 200 with multiple frame inputs 240]**, *each frame having a header and a data field* **[OC12, FE, and OC48 frames have both headers and a payloads]**, *for* deep packet processing *of the data field on each frame* in a given sequence **[e.g., deep packet processing such as encryption or compression, col. 9, lines 10-15 and col. 15, lines 9-11]**, performing the deep packet processing of data *fields* and forwarding the processed frames to their destination in the same given sequence **[the processing engine 300 maintains header (packet) sequence; col. 7, lines 49-57; BQU 210 also maintains sequence of packets and can accommodate latency of packets and even different data rates, col. 8, lines 39-46; for encryption operations, it is inherent the packets are delivered in the same sequence as they are received]**,comprising

a) an input buffer for receiving frames for processing, having a buffer capacity of at least twice the size of the largest frame size **[Fig. 2, each input port to router 200 has its own packet memory 220 and queue memory 235, col. 7, lines 46-52; in addition, BQU 210 (interpreted as the data moving unit), contains buffers for storing the packets prior to delivering them to processing engine 300, col. 7, lines 59-67; this is interpreted as having a input buffer capacity at least twice as large as the frame]**, said buffer incorporated into a Data Moving Unit **[Fig. 2, BQU 210; thus, BQU 210 (with internal buffers) as well as memories 230 and 235 are interpreted as incorporated into BQU 210]** ;

b) a Frame Header Processing Unit **[Figs. 2, 3, and 9; processing engine 300 (minus output header buffer 900) is interpreted as the frame header processing unit]** for determining the type of deep packet processing operation to be performed on each frame **[BQU 210 delivers the header to processing engine 300 over path 290, col. 8, lines 16-18; prior to**

sending the header (packet) to processing engine 300 over path 290, BQU 210 buffers the packet in packet memory 220, col. 8, lines 19-21; the processing unit 300 can perform processing on both headers and packets, col. 7, lines 49-52; thus processing engine 300 can perform encryption or compression on the header and/or payload of the packet (col. 9, lines 10-15 and col. 15, lines 9-11)];

c) a plurality of processing core engines **[Fig. 3, parallel arrayed processors PE 400, col. 9, lines 34-37]**, wherein each core engine has its own deep packet processing operation to be conducted on *the data field of* a frame **[each PE 400 performs processing such as encryption or compression on the payload of packets, col. 15, lines 9-20]**, and an associated memory for storing a frame assigned to the engine until the engine is free to perform a deep packet processing operation on the *data field of the* frame **[Figs. 2-3 and 7, each PE 400 has an input header buffer (IHB) 700 with buffer pairs 710, col. 12, lines 35-40; this is interpreted as having an input buffer capacity at least twice as large as the frame]**;

d) an arbitrator for assigning an ascending frame sequence number to each frame and for forwarding each frame to one of the core engines for deep-packet processing **[Fig. 2, Arbiter 255 implements a queuing policy for entry into the router 200, col. 8, lines 1-4; it is inherent that the frame sequence is maintained because of the disparate input sources; also, BQU 210 maintains the frame sequence to processing engine 300 because the frames are sent to processing engine 300 (see col. 7, lines 49-57), processed, and then sent back to BQU 210 for delivery to the proper output port (see col. 8, lines 41-42); for encryption operations, it is inherent the packets are delivered in the same sequence as they are received]**;

e) an output buffer for collecting each frame as it is processed by a core engine, said buffer having a buffer capacity of at least twice the size of the largest frame size **[Figs. 3 and 9, each PE 400 has an output header buffer 900 with buffer pairs 910, col. 14, lines 7-14; interpreted as having a buffer capacity at least twice as large as the frame; moreover, it is inherent that BQU 210 uses a similar scheme, internal buffers and packet memory 230 (also interpreted as having a input buffer capacity at least twice as large as the frame), for merging the modified header and/or packets prior to sending them to the output ports, col. 7, lines 62-67]** comprising a portion of the Data Moving Unit **[Fig. 2; processing engine 300 communicates with BQU 210 (interpreted as the data moving unit) over path 290 so that the modified packet can be delivered to the correct physical output port via line cards 240, col. 8, lines 29-40; the examiner interprets that the path 290 and output header buffer 900 (i.e., buffer pairs 910) as a portion of BQU 210]**; and

f) a sequencer for forwarding processed frames from the output buffer to their destination in the same order as they are received by the input buffer **[Fig. 3; BQU 210 maintains the sequencing of packets, col. 8, lines 41-42; for encryption operations, it is inherent the packets must be delivered in the same sequence as they are received]**.

5. The examiner believes that the buffers/queues disclosed in Key et al. are at least twice the capacity of the incoming/delivered frames. However, if it the capacities are not twice the size of the frames, Key et al. does disclose a data packet buffering system for use in a router **[Fig. 2; each input port to router 200 has its own packet memory 220 and queue memory 235, col. 7, lines 46-52; in addition, BQU 210 (interpreted as the data moving unit), contains buffers**

for storing the packets prior to delivering them to processing engine 300, col. 7, lines 59-67; Figs. 3 and 9, each PE 400 has an output header buffer 900 with buffer pairs 910, col. 14, lines 7-14; BQU 210 uses a similar scheme, internal buffers and packet memory 230, for merging the modified header and/or packets prior to sending them to the output ports, col. 7, lines 62-67]. Key et al. even uses FIFOs for memory **[col. 12, lines 35-40]**. Moreover, it is well know in the art to use FIFOs for buffering/queuing. Dockser discloses a packet FIFO that makes more effective use of a packet-data channel **[col. 1, lines 8-10]**. Dockser et al. also discloses that data packet buffering—such as greater-than-one-maximum-sized-packet capacity buffers—reduce packet latencies **[col. 2, lines 39-58]**. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the input and output buffers/queues of Key et al. to have a capacity of at least twice the largest frame received because such a double/triple/quadruple-sized buffer increases speed and efficiency **[col. 3, lines 5-7]** and makes better use of the data paths **[col.3, lines 40-43]**.

6. With regard to claim 22, Key et al. discloses a method of transmitting multiple frames **[Fig. 2, level 2/3 Router 200 with multiple frame inputs 240]**, *each frame having a header field and a data field* **[OC12, FE, and OC48 frames have both headers and a payloads]**, to deep packet processing functions in a given sequence **[e.g., deep packet processing such as encryption or compression, col. 9, lines 10-15 and col. 15, lines 9-11]**, performing the deep packet processing of data *field of each frame* and forwarding the processed frames to their destination in the same given sequence **[the processing engine 300 maintains header (packet) sequence; col. 7, lines 49-57; BQU 210 also maintains sequence of packets and can accommodate latency of**

packets and even different data rates, col. 8, lines 39-46; for encryption operations, it is inherent the packets are delivered in the same sequence as they are received], comprising the steps of:

a) receiving frames into an input buffer that is incorporated into a Data Moving Unit, said buffer having a buffer capacity of at least twice the size of the largest frame size to be processed **[Fig. 2, each input port to router 200 has its own packet memory 220 and queue memory 235, col. 7, lines 46-52; in addition, BQU 210 (interpreted as the data moving unit), contains buffers for storing the packets prior to delivering them to processing engine 300, col. 7, lines 59-67; this is interpreted as having a input buffer capacity at least twice as large as the frame]**;

b) *using a* Frame Header Processing Unit **[Figs. 2, 3, and 9; processing engine 300 (minus output header buffer 900) is interpreted as the frame header processing unit]** *to determine from the header field the type of deep packet processing operation to be performed on the data field of each frame* **[BQU 210 delivers the header to processing engine 300 over path 290, col. 8, lines 16-18; prior to sending the header (packet) to processing engine 300 over path 290, BQU 210 buffers the packet in packet memory 220, col. 8, lines 19-21; the processing unit 300 can perform processing on both headers and packets, col. 7, lines 49-52; thus processing engine 300 can perform encryption or compression on the header and/or payload of the packet (col. 9, lines 10-15 and col. 15, lines 9-11)]**;

c) assigning each frame to one of a plurality of processing core engines, based upon the processing operation to be conducted on the *data field of the* frame, each frame being stored in a memory associated with a core engine until the engine is free to perform the processing

operation on the *data field of the* frame; d) performing at least one deep-packet processing operation on the data *field* in each frame **[Fig. 2, Arbiter 255 implements a queuing policy for entry into the router 200, col. 8, lines 1-4; it is inherent that the frame sequence is maintained because of the disparate input sources; also, BQU 210 maintains the frame sequence to processing engine 300 because the frames are sent to processing engine 300 (see col. 7, lines 49-57), processed, and then sent back to BQU 210 for delivery to the proper output port (see col. 8, lines 41-42); for encryption operations, it is inherent the packets are delivered in the same sequence as they are received]**;

e) collecting the processed frames in an output buffer that is incorporated into a Data Moving Unit **[Fig. 2; processing engine 300 communicates with BQU 210 (interpreted as the data moving unit) over path 290 so that the modified packet can be delivered to the correct physical output port via line cards 240, col. 8, lines 29-40; the examiner interprets that the path 290 and output header buffer 900 (i.e., buffer pairs 910) as a portion of BQU 210]**, said buffer having a buffer capacity of at least twice the size of the largest frame size to be processed **[Figs. 3 and 9, each PE 400 has an output header buffer 900 with buffer pairs 910, col. 14, lines 7-14; interpreted as having a buffer capacity at least twice as large as the frame; moreover, it is inherent that BQU 210 uses a similar scheme, internal buffers and packet memory 230 (also interpreted as having a input buffer capacity at least twice as large as the frame), for merging the modified header and/or packets prior to sending them to the output ports, col. 7, lines 62-67]**; and

f) sequencing and forwarding processed frames to their destination in the same order as received into the input buffer **[Fig. 3; BQU 210 maintains the sequencing of packets, col. 8,**

lines 41-42; for encryption operations, it is inherent the packets must be delivered in the same sequence as they are received].

7. The examiner believes that the buffers/queues disclosed in Key et al. are at least twice the capacity of the incoming/delivered frames. However, if it the capacities are not twice the size of the frames, Key et al. does disclose a data packet buffering system for use in a router **[Fig. 2; each input port to router 200 has its own packet memory 220 and queue memory 235, col. 7, lines 46-52; in addition, BQU 210 (interpreted as the data moving unit), contains buffers for storing the packets prior to delivering them to processing engine 300, col. 7, lines 59-67; Figs. 3 and 9, each PE 400 has an output header buffer 900 with buffer pairs 910, col. 14, lines 7-14; BQU 210 uses a similar scheme, internal buffers and packet memory 230, for merging the modified header and/or packets prior to sending them to the output ports, col. 7, lines 62-67]**. Key et al. even uses FIFOs for memory **[col. 12, lines 35-40]**. Moreover, it is well know in the art to use FIFOs for buffering/queuing. Dockser discloses a packet FIFO that makes more effective use of a packet-data channel **[col. 1, lines 8-10]**. Dockser et al. also discloses that data packet buffering—such as greater-than-one-maximum-sized-packet capacity buffers—reduce packet latencies **[col. 2, lines 39-58]**. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the input and output buffers/queues of Key et al. to have a capacity of at least twice the largest frame received because such a double/triple/quadruple-sized buffer increases speed and efficiency **[col. 3, lines 5-7]** and makes better use of the data paths **[col.3, lines 40-43]**.

Response to Arguments

8. Applicant's arguments with respect to claims 21-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

(a) Tremblay et al. (USP 6205,543), Efficient handling of a large register file for context switching.

(b) Bunce et al. (USP 6,838,808), Pipelined packet processing.

(c) Georgiou et al. (USP 7,7072,970), Programmable network protocol handler architecture.

(d) Boutand (6,353,307), Data processing device with mask and status bits for selecting a set of status conditions.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Mais whose telephone number is 572-272-3138. The examiner can normally be reached on M-Th 5am-4pm.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan F. Wing can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MAM
May 30, 2007

CHI PHAM
SUPERVISORY PATENT EXAMINER
6/1/07